NIET Journal of Engineering & Technology (NIETJET)
Volume 11, Issue 1, 2020 ISSN: 2229-5828 (Print)

Analysis of Low Density Parity Check Code Decoder for Low Power Applications

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Abstract: *Because of its enough error detecting and repairing capabilities the low power, high efficient Low Density Parity-Check Code (LDPC) Decoder Architecture for error detection & correction applications. Low Density Parity-Check codes have been adopted in latest wireless standards such as satellite and mobile communications since they obtain superior error-detecting and correcting capabilities. However, as technology advances, building such a decoder has always been a challenge because it necessitates specific memory size and power consumptions. In this paper, we propose an LDPC decoder design by the use of Booth Algorithm that addresses these check in this study. The architecture was synthesized on Xilinx 14.7, and the synthesis report showed that the propose architecture uses less hardware and consumes less power than the conventional architecture, resulting in a more standard outcome.*

Keywords - LDPC, Booth Algorithm, Xilinx 14.7

INTRODUCTION:

In information theory, a low-density parity-check code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel. An Low Density Parity-Check is constructed using a sparse Tanner graph Low-density parity-check [1] codes are well-known for their high-speed data transfer proficiency and low complexity. However, binary LDPC codes of non-extreme or short duration have been shown to have an early error floor and poor decoding efficiency. These codes have been used in WiMAX and other high-speed applications, where parallel implementations of iterative message-passing algorithms are suitable for LDPC decoding. Reducing the algorithm's complexity reduces chip size and power usage while also increasing throughput. Due to this Min-Sum algorithm was used to solve the issue. LDPC codes are finding enhance use in applications requiring reliable and highly efficient information transfer over bandwidth-constrained or return-channel-constrained links in the presence of corrupting noise.

There are a kind of encoding algorithms that are commonly used. The Belief Propagation (BP) algorithm outperforms the others in terms of decoding. To compute the check node in the standard BP algorithm, various multiplicative and logarithmic computations are needed. The product word is swapped with the minimal value in the Min-Sum (MS) algorithm. Even though efficiency is diminished, the BP algorithm's hardware complexity is reduced dramatically by replacing complicated search node computations with basic summation and comparison operations. Under finite word-length implementations, the min-sum algorithm provides less sensitivity in decoding efficiency and does not require channel information.

We choose the Booth Algorithm [2] over the Belief Propagation Algorithm for our project because it can accommodate both positive and negative integers. When the multiplier has few big blocks of 1s and the speed is gained by skipping 1s, the Booth Algorithm achieves efficiency in the number of additions needed.

Related Works:

By reducing the quantization word length of decoding information and thereby decreasing hardware complexity, Yao et al. (2011) introduced the concept of a memory efficient LDPC decoder. By using shortword lengths with guaranteed Bit-Error-Rate, two quantization schemes were proposed to reduce the amount of memory bits needed by decoder design (BER). Their findings revealed that the two quantization schemes reduce hardware complexity while preserving decoding efficiency.

Swapna and Anbuselvi (2012) developed an LDPC decoder based on the wave pipelining principle, which

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reduces the decoding process' latency. This research revealed the internal architecture in depth, as well as the design complexity in terms of hardware utilisation variables.

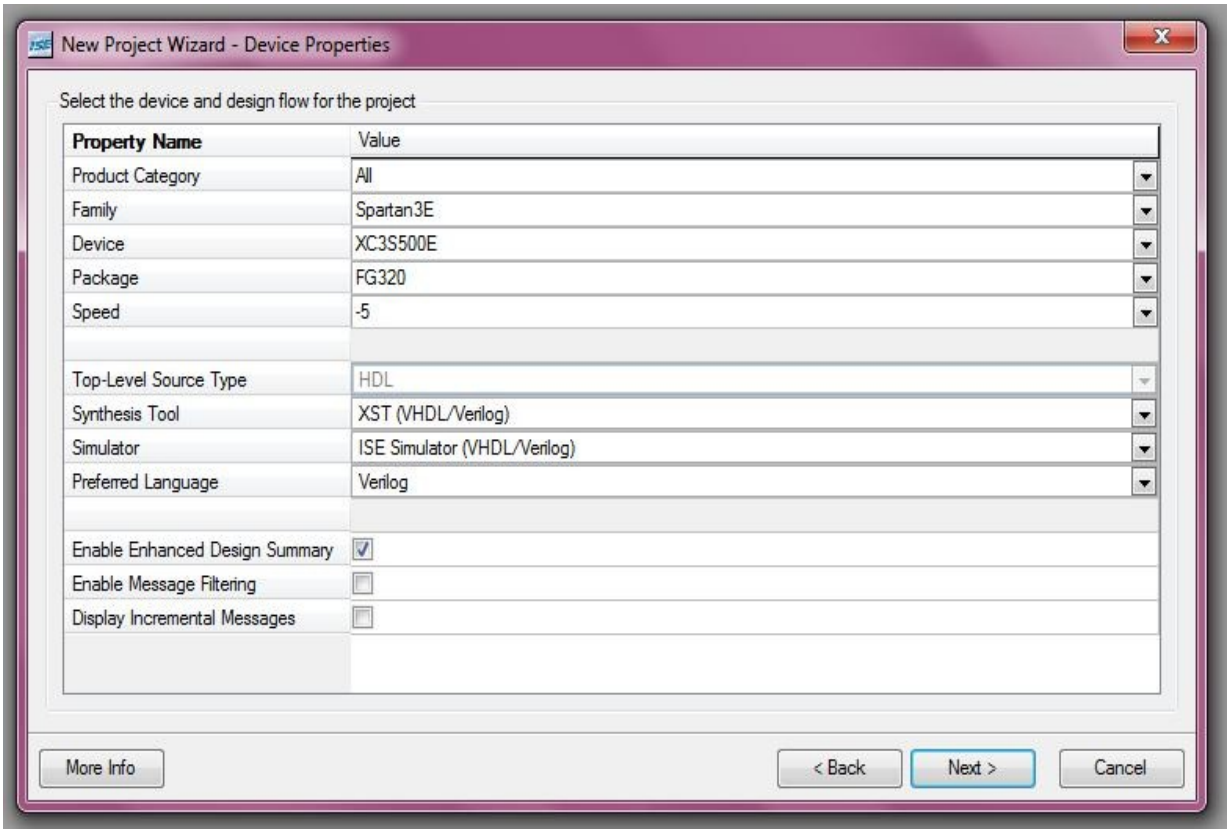
The serial GF(64)-LDPC decoder based on the Extended Min-Sum algorithm was proposed by Boutillon et al. (2013). For various code rates and lengths, their decoder architecture achieved a value of less than 0.7dB using the Belief Propagation algorithm. Their architecture adapts well to decoding extremely high Galois Field instructions, such as GF(4096) or higher.

In 2014, Revathy and Sarvanan proposed an LDPC architecture for error detection and correction applications that was low power and high performance. They reasoned that reducing algorithm complexitywould result in a smaller processor and therefore lower power consumption. As a result, they used the Belief Propagation algorithm, which provides excellent decoding results.. Control Node Unit and VariableNode Architecture were suggested as part of the decoder architecture. They then analysed and simulated the architecture. They concluded that the proposed LDPC decoder was well designed for low power applications that consumed a minimum of 81.37mW of energy based on their testing. Eventhough it provides low power consumption, the hardware complexity and area utilisation is high.

WORKING:

XILINX ISE TOOL FLOW:

The Integrated Software Environment (ISE) is that the Xilinx[3] design software suite that enables you to require the look from design entry through Xilinx device programming. The ISE Project Navigator manages and processes the planning through the subsequent steps within the ISE design flow.



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DESIGN ENTRY:

Design entry is that the initiative within the ISE design flow. During design entry, you create the source files supported the planning objectives. you'll create the top-level design file employing a Hardware Description Language (HDL), like VHDL, Verilog, or ABEL, or employing a schematic. you will be able to use multiple formats for the lower-level source files within the design. If work starts with a synthesized EDIF or NGC/NGO file, design entry and synthesis steps may be skipped and begin with the implementation process.

SYNTHESIS:

Formulation is run after concept entry and possible simulation. VHDL, Verilog, or mixed language prototypes are converted to netlist files, which are then passed onto implementation level.

IMPLEMENTATION:

After synthesis, you run design implementation, which converts the logical design into a physical file format that may be downloaded to the chosen target device. From Project Navigator, you'll run the implementation process in one step, otherwise you can run each of the implementation processes separately. Implementation processes vary reckoning on whether you're targeting a Field Programmable Gate Array (FPGA) or a fancy Programmable Logic Device (CPLD).

VERIFICATION:

You can verify the functionality of the planning at several points within the design flow. you'll be able to use simulator software to verify the functionality and timing of the planning or some of the look. The simulator interprets VHDL or Verilog code into circuit functionality and displays logical results of the described HDL to work out correct circuit operation. Simulation allows you to make and verify complex functions in an exceedingly relatively bit of your time. you'll be able to also run in-circuit verification after programming the device.

DEVICE CONFIGURATION:

You customize the system after creating a code file. During configuration, you generate configuration filesand download the programming files from a bunch computer to a Xilinx device. For transcription and FPGA execution of the 2D-DCT code interpreter, this by using the Xilinx ISE method. The device chosen is Spartan3 XC3S400.

Synthesis using Xilinx are often done by following steps:

1) Now create a replacement project and choose device Spartan3 and so XC3S400

2) Now add ASCII textfile.

3) Go to Implementation

4) Synthesis XST

5) Now to vary to Behavioral simulation

6) Run the ASCII textfile

CONCLUSION:

A high-throughput low-complexity decoder implementation for standardized LDPC codes is addressed throughout this project. An estimated layered decoding strategy has been investigated to allow pipelining

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technique for layered decoding strategy. The proposed decoder is expected to achieve well over 4.7 Gb/s decoding efficiency after 15 implementations.

FUTURE SCOPE:

Low-density parity-check (LDPC) code, an extremely promising near-optimal error correction code (ECC), is being widely well thought-out in next generation industry standards. LDPC code implementations are widely employed in DVB-S2, T2 or Wi-MAX standards. Unlike many other classes of codes, LDPC codes are already equipped with in no time (probabilistic) encoding and decoding algorithms. These algorithms can recover the initial codeword within the face of enormous amounts of noise. The iterative decoding approach is already employed in turbo codes but the structure of LDPC codes give better results. In many cases they permit a better code rate and a lower error floor rate. Furthermore, they create it possible to implement parallelizable decoders.

REFERENCES

[1] R. G. Gallager, „Low-Density Parity-Check Codes". Cambridge, MA: M.I.T. Press, 1963.

[2], Bernhard M.J. Leiner, LDPC Codes – a brief Tutorial Stud.ID.: 53418L bleiner@gmail.com,April 8 2005.

[3] Namrata P. Bhavsar, Brijesh Vala,„ Design of Hard and Soft Decision Decoding Algorithms of LDPC". International Journal of Computer Applications (0975 – 8887)

[4] Ashish Patil, Sushil Sonavane, Prof. D. P. Rathod, "Iterative Decoding schemes of LDPC codes", International Journal of Engineering Research and Applications (IJERA), March -April 2013.

[5] Sarah J. Johnson, „Introducing Low-Density Parity-Check Codes", School of Electrical Engineering and Computer Science, The University of Newcastle, Australia.

[6] William E Ryan, „ An introduction to LDPC codes", department of electrical and computer engineering. The University of Arizona,Australia,2003.

[7] M. Jadhav, ankit pancholi, dr. A. M. Sapkal,„Analysis and implementation of soft decision decoding algorithm of ldpc", pune university phase-i, d.-402, g.v 7, ambegaon, pune (india),[IJETT],2013.

[8] B. Vasic , Ivan B. Djordjevic, Low density parity check code and iterative decoding for long haul optical communication system,Journal of light wave technology , vol.21.no.2. February 2003

[9] Lakshmi.R, Tilty Tony, Abin Johns Raju, An Analytical Approach to The Performance of Low Density Parity Check Codes, International Conference on Advanced Computing and Communication Systems (ICACCS -2013), Dec. 19 21, 2013

[10] Vikram Arkalgud Chandrasetty, Syed Mahfuzul Aziz, FPGA Implementation of a LDPC Decoder using a Reduced Complexity Message Passing Algorithm , Journal of Networks, Vol. 6, no. 1, January 2011.

[11] Neelam, Pankaj Kumar, Atul Gupta; 'Routing Protocol in Mobile Network : A Review',Volume No.3,Issue No.2,2015,PP.045-052,ISSN :2229-5828

[12] Pawan Kumar Dubey, B. Mohpatra; 'Analysis of XPM-induced cross talk in the optical order dispersion with respect to power input to the fiber',Volume No.4,Issue No.2,2016,PP.001-005,ISSN :2229-5828

[13] Shukla, Ragini; 'Design Philosophy of Microwave Gunn Oscillator',Volume No.4,Issue No.2,2016,PP.006-009,ISSN :2229-5828

[14] Pritish Kulshreshtha, Sanjay Gairola And Anurag Verma; 'A Bi-DirectionalDC-DC Converter Feeding PMBLDC Motor Drive System',Volume No.4,Issue No.2,2016,PP.010-016,ISSN :2229-5828

Publisher: Noida Institute of Engineering & Technology,
19, Knowledge Park-II, Institutional Area, Greater Noida (UP), India.

[15] Vinay Kumar Dubey, Prabhaker Agarwal and V K Pandey; 'UHF RFID Reader Antena Using Double Slot Loaded Circular Patch',Volume No.4,Issue No.2,2016,PP.017-020,ISSN :2229-5828

[16] Sunil Kumar ,Kavita Kamboj, Manvi Tayal and Tanu Singh; 'Enhancing the Performance of Multi Area AGC in Deregulatd Enviroment Tuned with SSSC',Volume No.4,Issue No.2,2016,PP.021-026,ISSN :2229-5828

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19, Knowledge Park-II, Institutional Area, Greater Noida (UP), India.