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Design and Verification of Multiplier using carry look ahead adder

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Abstract : *A Multiplier using Carry Look Ahead Adders instead of full adders to implement the reduction of the bit product matrix into the two numbers that are added to make the product. Four-bit carry look Ahead adders are used in the reduction in place of individual full adders. Reduction of Nine partial products by a single carry look ahead adder (instead of 3 with a full adder) in same amount of time. This leads to fewer reduction stages than a traditional Wallace/Dadda Multiplier. One fewer stage is required for 4 by 4, 8 by 8, and 16 by 16 bit multipliers and 2 stages are saved for larger multipliers.*

Keywords -: Carry Look Ahead Adder, Full Adder, Wallace Multiplier, Dadda Multiplier

Introduction

A digital adder circuits are implemented using logic gates like OR, NOR, XOR, etc. These include half adders, full adders, parallel adders, carry-look ahead adders, and ripple-carry adders. The carry-look ahead adder, among all above is the fastest adder circuit. The binary addition of a large number of bits requires more time for the result to be generated. Using hardware circuitry of carry look ahead adder which is so complex, the propagation time is reduced, thus producing results much less than anticipated. The multiplier uses the addition arithmetic operation for all the partial products. The adder may be a carry-save adder, a ripple-carry adder, a carry-look-ahead adder, or any other adder. However, using a fast adder for the multiplier improves the overall performance of the multiplication operation. Carry Look Ahead Adder is generally used in many applications because of his speed enhancing properties. The purpose of using cla is enhancing the speed of a multiplier. Adder can be used for the design of add and shift multiplier which have lowest area, high speed and minimum power consumption.

Carry Look Ahead Adder: The ripple-carry adder, its limiting factor is the time it takes to propagate the carry. The Carry look-ahead adder solves this problem by calculating the carry signals in advance, based on the input signals. The result is a reduced carry propagation time.

To be able to understand how the carry look-ahead adder works, we have to manipulate the Boolean expression dealing with the full adder. The Propagate P and generate G in a Full-adder, is given as:

$Pi = Ai \oplus Bi$ Carry propagate

$Gi = AiBi$ Carry generate

Notice that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay.

The new expressions for the output sum and the carryout are given by:

$Si = Pi \oplus Ci\text{-}1$

$Ci+1 = Gi + PiCi$

These equations show that a carry signal will be generated in two cases:

1) If both bits Ai and Bi are 1

2) If either Ai or Bi is 1 and the carry-in Ci is 1.

Let's apply these equations for a 4-bit adder:

$C1 = G0 + P0C0$

$C2 = G1 + P1C1 = G1 + P1 (G0 + P0C0) = G1 + P1G0 + P1P0C0$

$C3 = G2 + P2C2 = G2 + P2G1 + P2P1G0 + P2P1P0C0$

$C4 = G3 + P3C3 = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C$

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BLOCK DIAGRAM OF CLA

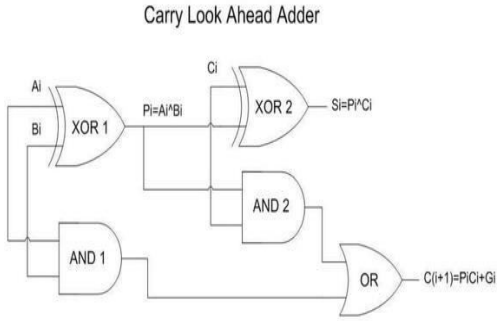

FIG.1 BLOCK DIAGRAM OF CARRY LOOK AHEAD ADDER

XILINX ISI SOFTWARE

Xilinx ISE is a discontinued software tool for synthesis and analysis of HLD designs, whose basic targets is development of flash memory chip for Xilinx FPGA and CPLD integrated circuit product families the functions ,take appropriate inputs manually and then the decisions accordingly.

HARDWARE USED: FPGA

FPGA stands I0f "Field Programmable Gate Array". FPGA is user-programmable interconnects used for operation of a specific application. It contains ten thousand to more than that logic gates with programmable interconnection. Programmable interconnections are available for users or designers to perform given functions easily. A visual model FPGA chip is shown in the given figure 2. The I/O blocks or internal hardware blocks are designed and numbered according to function. There are several Configurable Logic Blocks for each module of logic level composition.

CLB performs the logic operation given to the hld module. The inter connection between CLB and I/O blocks are made with the help of horizontal routing channels, vertical routing channels and PSM (Programmable Multiplexers). The number of CLB it contains only decides the complexity of FPGA. The functionality of CLB's and PSM are designed by VHDL or any other hardware descriptive language. After programming, CLB and PSM are placed on chip and connected with each other with routing channels.

Fig.2 FPGA Chip

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WORKING

The carry look ahead adders in this paper are constructed with 2-input to 4-input AND,OR gates and inverters. Each gate is assumed to have one gate delay and counts as one gate for complexity. 4 modified full adders and one 4bit look ahead logic block are used to construct CLA4s. A CLA4 takes 6 gate delays from any input to any output and has a complexity of 42 gates.

CONCLUSION

Two different multipliers using a fast carry-look-ahead adder and a ripple adder have been modeled and simulated using VHDL. The multiplier with a carry-look-ahead adder shows a better performance over the multiplier with a ripple adder in terms of gate delays. In other words, the multiplier with the carry-look-ahead adder has approximately twice the speed of the multiplier with the ripple adder. Also, the multiplier with the carry-look-ahead adder uses less time.

FUTURE SCOPE

The proposed design can be modified by changing each stage of full adder with carry look ahead adder speed can be increased nearly up to 60% but this is possible at the cost of some tradeoff between area and power.

REFERENCES

[1] Mohita Sharma, Himanshu Josh, "Optimization and Analysis area of Carry look Ahead Adder" 2014 (IJAERS) (2349-6495) [Vol-1, Issue-1]
[2] Sai Bhavya, Mahesh Kumar, "Design of High Speed Multiplier by using Carry Select Adder"2018 (Volume 4, Issue 3)
[3] Shiwani Dod, "Modified Booth Dadda Multiplier Using Carry Look Ahead Adder Design and Implementation" Vol 7-Issue3 -2016
[4] T. Srinivasa Padmaja, C.M. Sri Priya, "Design and Implementation of Carry Look Ahead Adder in Quantum Dot Cellular Automata" Vol 3-Issue5-2018.
[5] Sunil Kumar ,Kavita Kamboj, Manvi Tayal and Tanu Singh; 'Enhancing the Performance of Multi Area AGC in Deregulatd Enviroment Tuned with SSSC',Volume No.4,Issue No.2,2016,PP.021-026,ISSN :2229-5828
[6] Nidhi Sharma ,Raman Chauhan, Sudhanshu AggarwaL; 'An Analysis of Utilization Factor of Fee- Counter in Colleges',Volume No.4,Issue No.2,2016,PP.027-030,ISSN :2229-5828
[7] Sudhanshu Aggarwal , Raman Chauhan, Nidhi Sharma; 'Solution of Linear Voltera Integro -Differential Equations of Second Kind by Using Laplace Decomposition Algorithm',Volume No.4,Issue No.2,2016,PP.031-034,ISSN :2229-5828
[8] Rahul kumar Sharma , Mayank Deep Khare , Amrendra Singh Yadav, Ayushi Singhal; 'Evaluation of Latency in Delay Sensitive Cloud Services',Volume No.4,Issue No.2,2016,PP.035-039,ISSN :2229-5828
[9] Amrendra Singh Yadav , Ayushi Singhal , Rahul kumar Sharma, Mayank Deep Khare; 'An optimized approach over hybrid scheme through removing unidirectional links',Volume No.4,Issue No.2,2016,PP.040-043,ISSN :2229-5828
[10] Ayushi Singhal , Amrendra Singh Yadav ,Mayank Deep Khare, Rahul Kumar Sharma; 'Integrated MANET Mutual Authen-tication System -A Review',Volume No.4,Issue No.2,2016,PP.044-052,ISSN :2229-5828
[11] Jitendra Kumar Saroj, V.K.Pandey; 'Micro -strip Slot Antenna with High Efficiency',Volume No.4,Issue No.2,2016,PP.053-056,ISSN :2229-5828

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