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DESIGN OF PHASE COMPENSATION CIRCUITS FOR MULTISTAGE OP-AMP

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Abstract

The technique of compensation is used to provide stability to rather unstable systems, which become so due to obvious use of the closed loop feedback. The capacitor in feedback path that decreases the flow of current through main feed forward path at various frequencies, causes the path of low reactance in feedback loop. This effect introduces the phase error within the circuit. In this paper compensation strategy has been simulated to overcome this effect. Simulation result shows an improvement upto 35 degrees.

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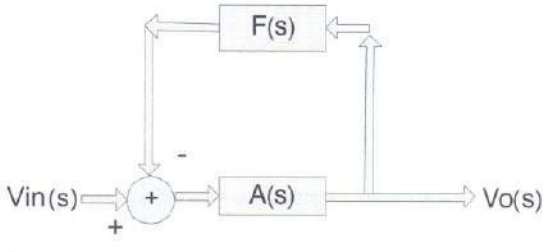
Introduction

The general configuration that is used for the application of the op-amp is closed loop. It is to use the relatively high, inaccurate forward gain with feedback for achieving a highly accurate transfer function which is in turn the function of feedback elements only. The figure below depicts the negative feedback configuration. The amplifier gain is the open loop, differential voltage gain denoted by A(s). The transfer function for the feedback is F(s). The system loop gain is given by

Loop Gain, L(s) = -A(s)F(s)

The utmost requirement here is that the signal fed back to the input of the op-amp be of such amplitude and phase that it does not keep regenerating itself around the loop. The equation for this requirement is as below:-



$$|A(j\omega_0')F(j\omega_0')| = |L(j\omega_0')| < 1$$

here ω_0' is defined as, Arg[-$A(j\omega_0')F(j\omega_0')$ Arg $L(j\omega_0') = 0°$

If the above condition is met, then the feedback system is stable i.e. sustained oscillation cannot occur. The requirement for stability is that the $|A(j\omega)F(j\omega)|$ curve crosses the 0 dB point before the $Arg[-A(j\omega)F(j\omega)]$ reaches 0°. A measure of stability is given by the value of the phase when $|A(j\omega)F(j\omega)|$ is unity, 0 dB. This measure is called the phase margin and is described by the following relationship:

Phase Margin, $\varphi M = Arg[-A(j\omega\_(0\ dB))\ F(j\omega\_(0\ dB))] = Arg[L(j\omega\_(0\ dB))]$

Compensation technique used

The compensation technique is employed in the multistage (two and three stage) op-amp here. Let gmI , gmII and gmIII be the respective transconductances of two stage and three stage op-amps here. This technique is applied by connecting a capacitor from the output to the input of the second transconductance stage. The resulting small signal model for the two stage case is depicted in the figure below:-

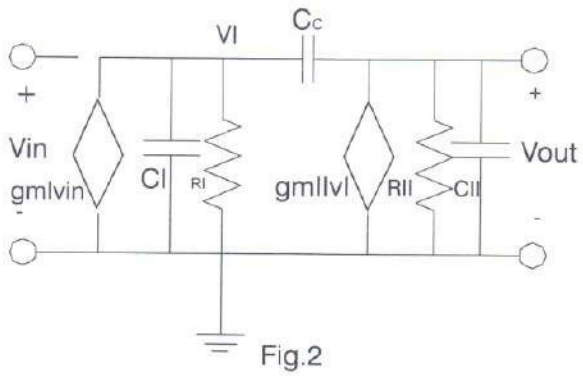


Fig.2

Two results are evident from adding the compensation capacitor CC. First, the effective capacitance shunting RI is increased by the additive amount of approximately gmIIRIICC. This moves pole p1 closer to the origin of complex frequency plane by a significant amount. Second, pole p2 is moved away from the origin of the complex frequency plane, resulting from the negative feedback reducing the output resistance of the second stage. The two compensated poles are given as below:-

$$p1 \cong \frac{(-1)}{g_{mII} R_I R_{II} C_C}$$

and

$$P_2 \cong \frac{-g_{mII} C_C}{C_I C_{II} + CI C_C + C_C CII}$$

In case, if CII is much greater than C_I and if C_C is greater than C_{II}, then above equation becomes as below:-

$$P_2 \cong \frac{-gm_{II}}{C_{II}}$$

It is to be noted here that a zero occurs on the positive real axis of the complex frequency plane and is due to the feedforward path through C_C. The right half plane zero is located at:

$$Z_1 = \frac{gm_{II}}{C_C}$$

The figure below shows the two stage and three stage cmos op-amps with the compensation. The next section includes the simulations and the results.

Simulation and Results

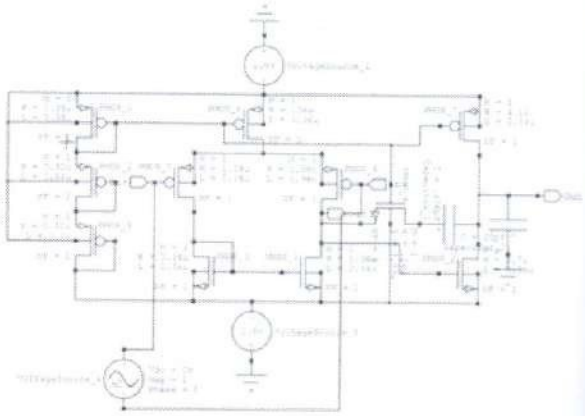
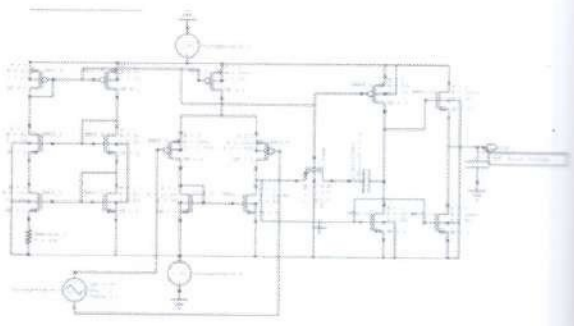


Fig.3 Two stage CMOS op-amp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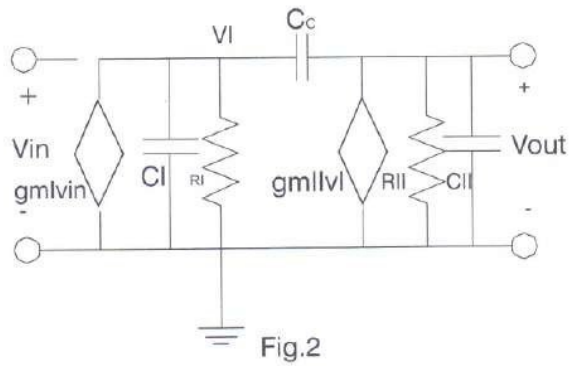

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Simulation and Results

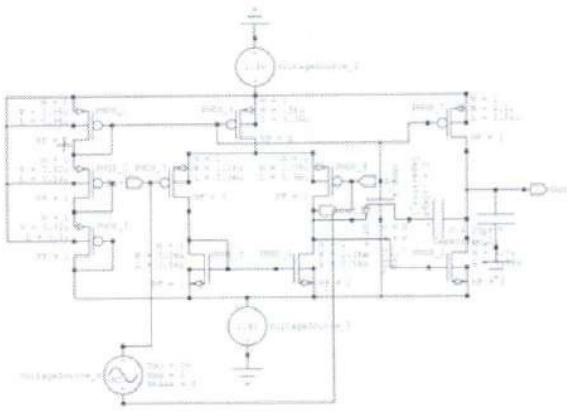
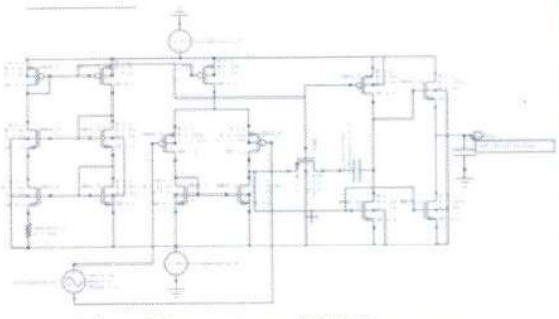


Fig.3 Two stage CMOS op-amp



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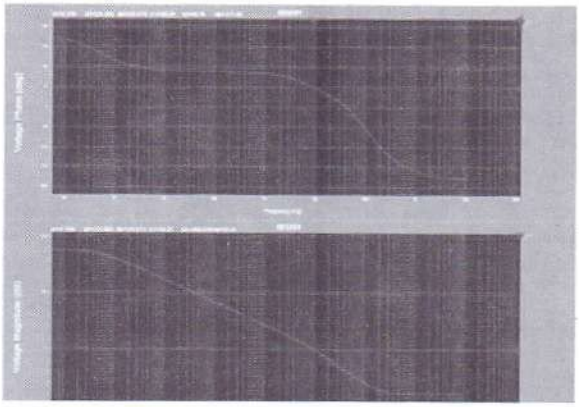

Fig.5 Simulation result for two stage op-amp

The fig.5 shows the simulation result for circuit shown in fig.3. The phase margin is 50°, which is in the stability criteria.

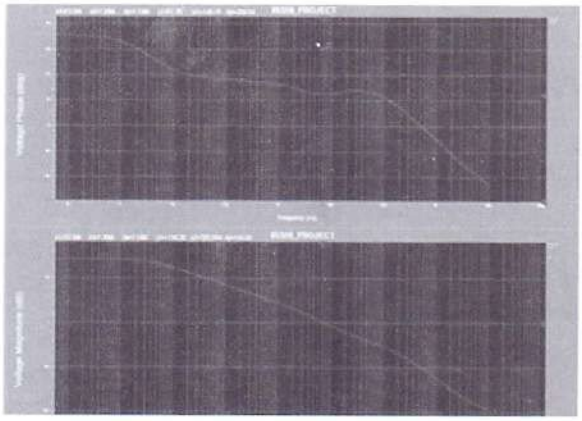

Fig.6 Simulation result for three stage op-amp

The fig.6 shows the simulation result for circuit shown in fig.4. The phase margin is 60°, improved and within the stability criteria.

Conclusion

The simulation results above show that the phase error has been reduced upto the required range. The phase margin is seen to be within the range of 45° - 60° which is the desired criteria for circuit stability. However, the reduction in phase margin causes decrease in the bandwidth of the circuit. This could be the future improvement aspect of the paper.

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