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VHDL IMPLEMENTATION OF INTERLEAVERS: FUNDAMENTALS AND RECENT DEVELOPMENTS FOR WIMAX AND WLAN

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Abstract

In this age of wireless communication, WLAN and WiMax are the most common IEEE standards used for wireless. The concept of OFDM is used in these standards to obtain a high data rate in addition to reducing the effects like inter symbol interference and inter channel interference. It has proved to be the air interface for the next generation Broadband Wireless System. FEC is a widely used technique to reduce the error. Interleaver is an important and powerful technique to combat a burst of errors for FEC coded signal. In this paper, different inter-leaver schemes which are implemented using VHDL on FPGA platform with all code rates and modulation schemes have been reviewed in relation to their fundamental application and challenges.

Keywords: *BWA, BER, WIMAX, WLAN, FEC, EEC, OFDM*

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Introduction

Growth of high-performance wireless communication systems has drastically increased over the last few years [1-2]. Due to rapid advancements and changes in radio communication systems, there is always a need for flexible and general purpose solutions for processing the data[3].Broadband Wireless Access (BWA) has become the most important and challenging segment of the wireless revolution since it is a viable alternative to the cable modem and digital subscriber line [4-6]. High processing speed, design flexibility and fast design Turn around Time (TAT) are the important requirements of BWA to meet the challenges posed to it [7-9]. To meet these requirements the designers choose the flexible VHDL and reconfigurable hardware platform like Field Programmable Gate Array(FPGA) [10-12].

Orthogonal Frequency Division Multiplexing (OFDM) technique offers a promising solution that has gained tremendous research interest in recent years due to its high transmission capability and also for alleviating the adverse effects of Inter Symbol Interference (ISI) and Inter Channel Interference (ICI)[13-14]. In an OFDM system, the data is divided into multiple parallel sub-streams at a reduced rate and each is modulated and transmitted on a separate orthogonal subcarrier [15-17]. This increases symbol duration and improves system

robustness [18-19]. OFDM is achieved by providing multiplexing on users' data streams on both uplink and downlink transmissions [20]. OFDM is the fundamental building block of the different IEEE wireless standards [21]. The main function of a communication system is to transmit information from the Source to the destination with sufficient reliability. The error correction codes (ECC) play a very important role in modern digital communication systems. Interleaving is an important and powerful technique to combat burst of errors for FEC coded signal. This technique is traditionally used to reduce the bit error rate (BER) of digital transmission over a bursty channel. An interleaver takes a given sequence of symbols and permutes their positions, arranging them in a different temporary order. The basic goal of an interleaver is to randomize the data sequence. When used against burst errors, interleavers are designed to convert error patterns that contain long sequences of serial erroneous data into a more random error pattern, thus they distributes errors among many code vectors. Interleavers are classified into two broad types: periodic interleaver and pseudo-random interleaver. In periodic interleaver, symbols of the transmitted sequence are scrambled as a periodic function of time .The two main classes of periodic interleaving are: block interleaving and convolutional interleaving. Pseudo-random interleaver rearranges the data in a pseudo-random sequence. The principal aim of this work is to review the efficient VHDL implementation of convolutional interleaver and block interleaver for common OFDM based IEEE standards like WLAN and WiMax which leads to higher operating frequency, better resource utilization, lower power consumption and reduced delay in the interconnection network.

The rest of the paper is organized as follows: section II presents the detail of interleaving in digital data communication. Section III describes basics of convolutional interleaver. Section IV describes the proposed hardware model of the efficient convolutional interleaver. Section V describes basics of block interleaver. Section VI describes the proposed hardware model of the FSM based block interleaver for WLAN. Section VII describes the proposed hardware model of the block interleaver for WiMax. Section VIII describes critical analysis of FPGA implementation. Concluding remarks are given in Section IX.

II. INTERLEAVING

Interleaving is a tool that can be used in digital communications systems to enhance the random error correcting capabilities of block codes. The interleaver subsystem rearranges the encoded symbols over multiple code blocks. This effectively spreads out long burst noise sequences so they appear to the decoder as independent random symbol errors or shorter, more manageable burst errors. The amount of error protection based on the length of the noise bursts determines the span length or depth of interleaving required.

Interleaving can be classified as either periodic or pseudo-random. The periodic interleaver orders the data in a repeating sequence of bytes. The two main classes of periodic interleaving are: block interleaving and convolutional interleaving [22]. The block Interleaver orders the data in a repeating sequence of bytes. The two main classes of periodic interleaving are: block interleaving and convolutional interleaving [22]. The block interleaver accepts symbols in blocks and performs identical permutations over each block of data. One way this is accomplished involves taking the input data and writing the symbols by rows into a matrix with i rows and n columns and then reading the data out of the matrix by columns. This is referred to as a (n,i) block interleaver and in convolutional interleaver the code word symbol from the encoder is fed into the array of shift registers, one code symbol to each row. With each new code word symbol the commutator switches to a new register and the new code symbol is shifted out to the channel. Pseudo-random interleaver rearranges the data in a pseudo-random sequence. Periodic interleaving is more commonly invoked because it is more easily accomplished in hardware.

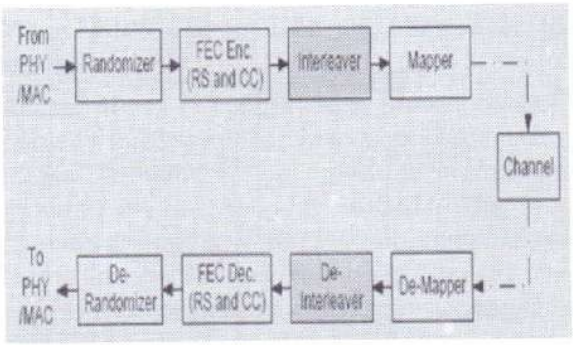

Fig.1.Communication system (WiMax PHY layer).

III. Convolutional interleaver

A convolutional interleaver consists of N rows of shift registers, with different delay in each row. In general, each successive row has a delay which is J symbols duration higher than the previous row. The code word symbol from the encoder is fed into the array of shift registers, one code symbol to each row. With each new code word symbol the commutator switches to a new register and the new code symbol is shifted out to the channel. The i-th ($1 \leq i \leq N-1$) shift register has a length of (i-1)J stages where J = M/N and the last row has M-1 numbers of delay elements[23]. The convolutional deinterleaver performs the inverse operation of the interleaver and differs in structure of the arrangement of delay elements. Zeroth row of interleaver becomes the N-1 row in the deinterleaver. 1st row of the former becomes N-2 row of later and so on.

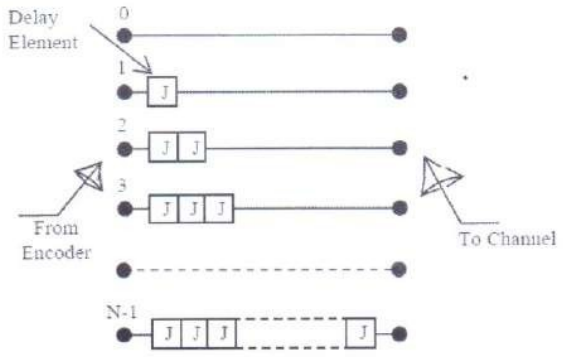

FIG.2. Convolutional interleaver

IV. Proposed model of convolutional interleaver

The proposed VHDL model of an 8 bit Convolutional interleaver with J = 1 is presented in Fig. 3. The code word symbols (Din) received in serial form from an encoder is converted into an 8 bit parallel code word by a Serial Input Parallel Output (SIPO) register. The SIPO output changes its value with each clock which is not desirable at the input of the delay unit. The buffer unit delivers a word to the delay unit after every 8 Clock cycles. The delay unit is comprised of eight rows and is having the structure as narrated in Fig. 2[24]. Each code symbol of the 8 bit code word is applied to the respective row of the delay unit. The code word gets scrambled as it progresses through the delay unit. The scrambled code word then applied to the input of an 8 line to 1 line multiplexer (MUX) which converts it into a stream of serial data (Dout)[25][26]. The interleaver circuit requires a clock signal to drive the SIPO register; a clock circuit and a three bit counter [27]. The clock circuit basically divides the system clock frequency by 8 which is used to drive the buffer and delay unit[28]. The 3 bit counter generates the select input for the MUX[29].

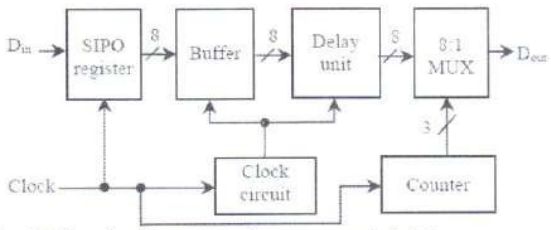

Fig.3 Block diagram of proposed 8 bit convolutional interleaver.

V. Basics of block interleaver

The block interleaver is loaded row by row with L codewords, each of length n bits. These L code words are then transmitted column by column until the interleaver is emptied. Then the interleaver is loaded again and the cycle repeats. At the receiver, the codewords are deinterleaved before they are decoded. A burst of length L bits or less will cause no more than 1 bit error in any one codeword. The random error decoder is much more likely to correct this single error than the entire burst. The parameter L is called the interleaver depth. The interleaver depth is chosen based on worst case channel conditions. It must be large enough so that the interleaved code can handle the longest error

bursts expected on the channel. The main drawback of block interleavers is the delay introduced with each row-by-row fill of the interleaver.

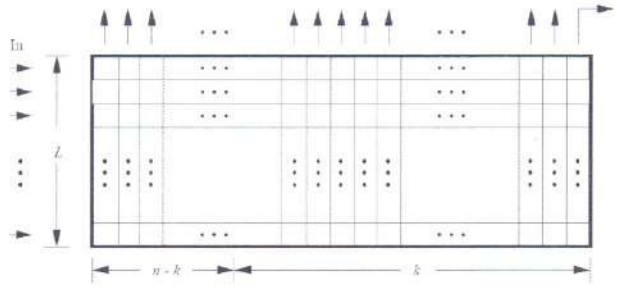

Fig 4 Block interleaver

VI. Hardware model of interleaver for wlan.

The proposed hardware model of OFDM based WLAN interleaver consists of two sections: address generator and interleaver memory.

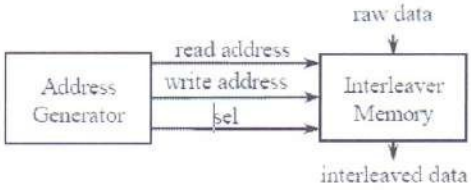

Fig 5. Top level view of interleaver

A.Address generator

Our proposed design of address generator block is described in the form of schematic diagram in Fig. 6[30]. Bulk of the circuitry is used for generation of write address. It contains three multiplexers (muxs): mux-1 and mux-2 implements the unequal increments required in 16-QAM and 64-QAM whereas mux-3 routes the outputs received from mux-1 and mux-2 along with equal increments of BPSC and QPSK. The select input of mux-1 is driven by a T-flipflop named qam16_sel whereas that of mux-2 is controlled by a mod-3 counter, qam64_sel. The two lines of mod_typ (modulation type are used as select input of mux-3. The 6-bit output from the mux-3 acts as one input of the 9-bit adder after zero padding. The other input of the adder comes from accumulator, which holds the previous address. After addition a new address is written in the accumulator.The preset logic is a

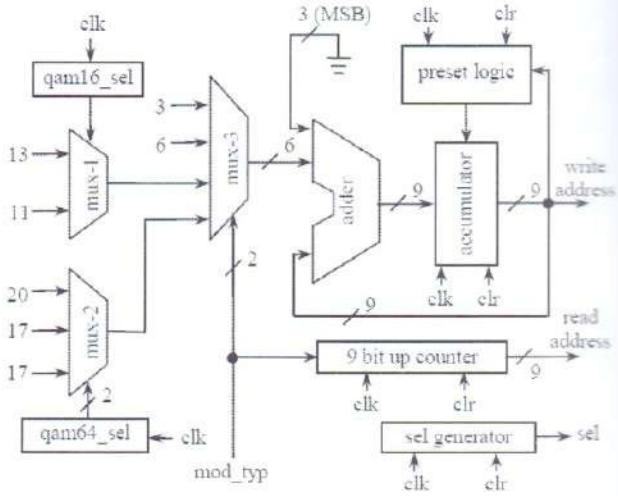

Fig 6. Schematic diagram of address generator

hierarchical FSM whose principal function is to generate the correct beginning addresses for all subsequent iterations. This is presented in reference .

B. Interleaver memory

The interleaver memory block comprises of two memory modules (RAM-1 and RAM-2), three muxs and an inverter as shown in Fig. 7. In block interleaving when one memory block is being written the other one is read and vice-versa. Each memory module receives either write address or read address with the help of the mux connected to their address inputs (A) and sel line. RAM-1 at the beginning receives the read address and RAM-2 gets the write address with write enable (WE) signal of RAM-2 active. After a particular memory block is read / written up to the desired location, the status of sel changes and the operation is reversed. The multiplexer at the output of the memory modules routes the interleaved data stream from the read memory block to the output.

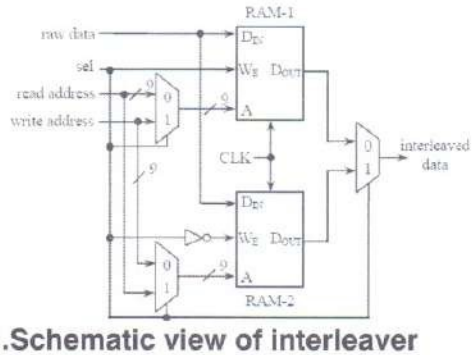

FIG 7.Schematic view of interleaver Memory block.

VII. HARDWARE MODEL OF Interleaver for wimax

As shown in Fig.8 [31], the design concept contains three levels of multiplexer. The first level MUXs implement the unequal increments required in 16-QAM and 64-QAM. The four-interleaver depths of 16-QAM are implemented by the first four MUXs from the top in level 1. The select inputs of these four MUXs are tied together and are driven by a T-flip flop named QAM16_SEL. Similarly, the last four MUXs are for 64-QAM modulation. The select inputs are driven by a mod-3 counter - QAM64_SEL. The second level MUXs basically pick up one input based on the values of ID [32]. The topmost MUX in level 2 implements the eight interleaver depths of QPSK modulation scheme available by concatenation of sub-channels. The second and third MUXs in level 2 are for 16-QAM and 64-QAM respectively. The outputs from level 2 MUXs are routed to the next section by level 3 MUX based on MOD_TYP value[33]. The 7-bit output from the level 3 MUX acts as one input to the 10-bit adder circuit after zero padding. The other input of the adder comes from the Accumulator, which holds the previous address. After addition a new address is written in the Accumulator [34]. The preset logic is a FSM whose principal function is to generate the correct beginning addresses for all subsequent iterations [35].

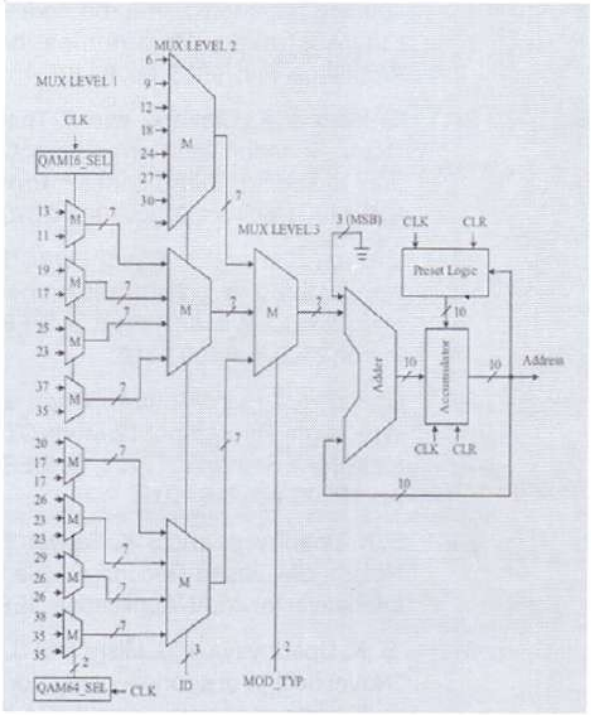

Fig 8 . Address generation scheme.

VIII. Critical analysis of fpga implementation

The proposed VHDL model of the interleaver is prepared using Xilinx Integrated Software Environment (ISE) [36-37] and is implemented on Xilinx Spartan-3 FPGA[38-39]. Simulation result of the proposed interleaver for OFDM based WLAN and WIMAX is presented in the form of timing diagram [40-41].

IX. Conclusion

In this paper an efficient VHDL model of the Convolutional and FSM based block interleaver for WLAN and WIMAX are reviewed. Simulation result has been taken from different literature. Both interleaver techniques reduce FPGA resource utilization, less power consumption, reduced FPGA interconnection delays and lower memory wastage compared to popular implementation techniques.

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In case of Tridax procumbens the synergistic analgesic effect showed significance with as less as 50 mg / kg, p.o. of Ibuprofen. But with less than 50 mg/kg, p.o. the synergistic effect of Tridax procumbens was insignificant. In the analgesic model, the analgesic effect of the herb was highest in the 2nd hr. But, when Ibuprofen was added the highest analgesic effect was seen in the 1st hr (due to the action of Ibuprofen).

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Basu Saumya P and Das Manas K,
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